Lifting Based Discrete Wavelet Transform Architecture for JPEG2000

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ABSTRACT

A lifting based 1-D Discrete Wavelet Transform (DWT) core is proposed. It is re-configurable for 5/3 and 9/7 filters in JPEG2000. Folded architecture is adopted to reduce the hardware cost and achieve the higher hardware utilization. Multiplication is realized in hardwired multiplier with coefficients represented in canonic signed-digit (CSD) form. It is a compact and efficient DWT core for the hardware implementation of JPEG2000 encoder.

1. INTRODUCTION

There has been a long history of the development of wavelet transform [1]. After the demonstration of the fingerprinting standard, which is the co-operation of FBI in the US and NIST, the use of wavelet technology as the transform core for image processing gains considerable interest. Discrete wavelet transform is now adopted to be the transform coder in both JPEG2000 [2] still image coding and MPEG-4 [3] still texture coding. In this paper, we mainly focus on the design of the 1-D DWT core for JPEG2000.

JPEG2000 is the emerging next generation still image compression standard. Part one (the core) of JPEG2000 is to be delivered and agreed as a full ISO International Standard by the end of the year 2000. With the inherent features of wavelet transform, it provides multi-resolution functionality, and better compression performance at very low bit-rate compared with the DCT-based JPEG [4] standard. To provide efficient lossy and lossless compression within a single coding architecture, two wavelet transform kernels are provided in part one of JPEG2000. The 5/3 reversible and 9/7 irreversible filters are chosen for lossless and lossy compression, respectively. A compact architecture for both 5/3 and 9/7 filter operation is, therefore, necessary for this unified hardware implementation. A number of architectures of DWT based on the classical implementation have been proposed in the literature [4]. As the newly proposed lifting-scheme [5-7] for the computation of DWT has lower computational complexity than the classical implementation, we propose a folded architecture of 1-D DWT core based on the lifting scheme. It is re-configurable for 5/3 and 9/7 filters for the efficient implementation of JPEG2000 encoder.

This paper is organized as follows. In Section 2, the lifting scheme algorithm is described and compared with the classical implementation. The proposed 1-D DWT architecture is depicted in Section 3, and the 2-D DWT architecture based on the 1-D DWT core is also discussed. Finally, a conclusion is given in Section 4.

2. LIFTING SCHEME

Fig. 1 shows the classical implementation and the lifting based implementation of DWT. Classical implementation is realized by the convolution of the input signals with the low pass filter (h_0) and the high pass filter (h_1). The convolution kernels of 5/3 and 9/7 filters [9] in JPEG2000 are given in Table I, and Table II. Both of them are linear phase (symmetrical) filters. Lifting scheme is an alternative approach for the computation of the discrete wavelet transform. The block diagram in Fig. 1(b) depicted the three steps of lifting scheme. It begins with a trivial wavelet, the "Lazy wavelet", in split phase to split the data into two smaller subsets, even and odd. Then in the second phase, even samples multiplied by the prediction operator are used to predict the odd samples. The difference between the odd sample and the prediction value is the detail coefficient (d_j). In the third phase, even samples are updated with detail to get smooth coefficient (S_j). More algorithm details can be found in the original papers of lifting scheme [5-7].

The direct mapping of the lifting scheme to the hardware architecture is depicted in Fig. 2. Fig. 2(a) is the mapping for 5x3 filter, and Fig. 2(b) is for 9x7 filter. There is only one stage (one predict and one update) for the 5/3 filter, but there are two stages for 9/7 filter.

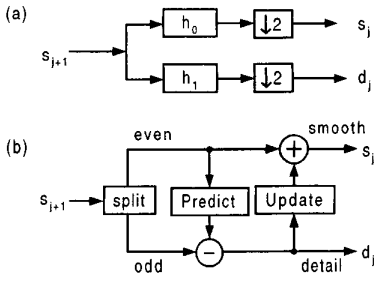

Fig. 1. Wavelet Transform: (a) classical implementation. (b) lifting-based implementation

Table I
Coefficients of the Daubechies (9,7) Filter

i	h_0	h_1
0	0.6029490182363579	1.115087052456994
1	0.2668641184428723	-0.5912717631142470
2	-0.07822326652898785	-0.05754352622849957
3	-0.01686411844287495	0.09127176311424948
4	0.02674875741080976	

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Table II
Coefficients of the Integer (5,3) Filter

i	h_0	h_1
0	6/8	1
1	2/8	-1/2
2	-1/8	

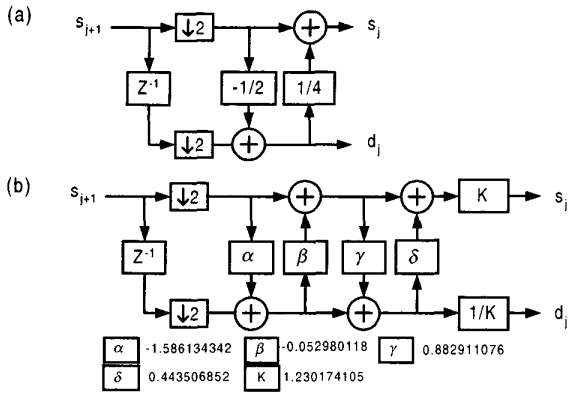

Fig. 2. Lifting-based implementation: (a) 5/3 filter architecture. (b) 9/7 filter architecture

There are some significant features of lifting scheme. First, by using the similarities between the high and low pass filters, the computation complexity is lower than traditional two-band subband transform scheme. The number of multiplications and additions needed for two points 5/3 and 9/7 1-D DWT by convolution and lifting scheme respectively are listed in Table III for comparison.

Table III
Complexity comparison of convolution and lifting-based implementation

	Two pixels 1-level 1-D DWT			
	Convolution		Lifting Scheme	
Filter	Multiplications	Additions	Multiplications	Additions
5/3	4	6	2	4
9/7	9	14	6	8

For a N×N image, decomposed into L levels, the computation complexity of lifting scheme is $N^2+N^2/4+N^2/16+.....+N^2/(4)^{L-1}$ multiplications, and $2\times(N^2+N^2/4+N^2/16+.....+N^2/(4)^{L-1})$ additions for 5x3 filter. Second, the lifting scheme allows in-place computation of the wavelet transform. The original signal will not be used for further computation and, therefore, can be replaced with the calculated wavelet transform coefficient. Third, no explicit boundary extension is needed. The symmetry mirroring effect is achieved by a multiplied-by-two operation at proper boundary positions.

It is feasible to calculating both 5/3 and 9/7 filter using the architecture in Fig. 3. It is proposed in [10] and redrawn here for illustration. The computation of 5/3 filter can be done by alternating the coefficients needed for 5/3 filter, and by taking the output from the first stage. However, the hardware utilization is only 50% when calculating 5/3 filter using this architecture. Also, provided only single read port and single write port memory is available, samples come in serially one sample per cycle and buffered, and then enter the DWT core two samples every other cycle. The hardware utilization is 50% lower due to the sub-sampling effect.

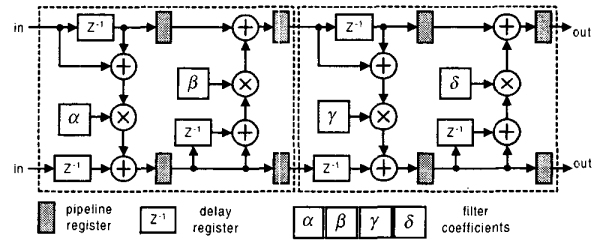

Fig. 3. Lifting based DWT architecture proposed in [10]

3. PROPOSED ARCHITECTURE

3.1 1-D DWT Architecture

To solve the problem of hardware in-efficiency described in the preceding section, a folded re-configurable 1-D DWT core is proposed. The detailed architecture is shown in Fig. 4.

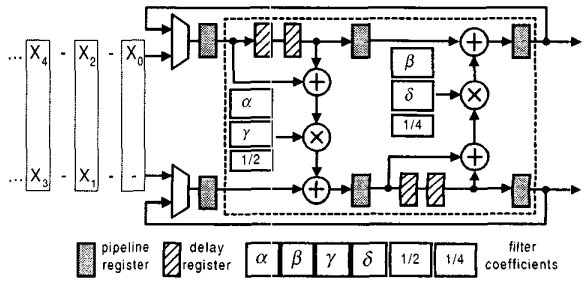

Fig. 4. Proposed folded architecture for 5/3 and 9/7 filter of DWT

Under the assumption that only single read port and write port memory is available, and only single-phase clock signal is used for the system, data read from memory one per cycle, and write back one per cycle. In the split phase of lifting scheme, the data are inputted into two shift registers, and two samples are read into the predict stage every other cycles. At the output, two output data are available in every other cycle, and a parallel to serial circuit is also added for the constraint on single write port memory. That means the input and output data rate to the DWT core are both one sample per clock cycle.

In the 9/7 filter mode, there are two stages of predict and update operation. Data after the first stage computation are feedback (folded) to R1 in Fig. 5 for the second stage computation. The computation of the first stage and the second one are interleaved. The hardware utilization is 100%. While in the 5/3 filter mode, no folded computing is necessary sine there is only one stage for lifting based operation for 5/3 filter. Another

difference is that the multiplication in 5/3 filter is in fact only shift-rigtht operation. More specifically, since for JPEG 2000, the filter coefficients are fixed. The number of bits to be shifted right is a constant, and only hardwired shifting with sign bit extension is necessary. The computation load in 5/3 is much lower than in 9/7. Also, since no interleaving computation of two stages exists in 5/3 mode, the computation time in predict and update phase can be equivalently two times of the clock period. Therefore, the pipeline registers of R2 and R3 in Fig.5 can be bypassed in 5/3 filter mode, with the effect that the latency is reduced without increasing the clock frequency. Fig. 6 illustrated the interleaving operation in 9/7 filter mode. The delay registers are ignored here for ease of explanation.

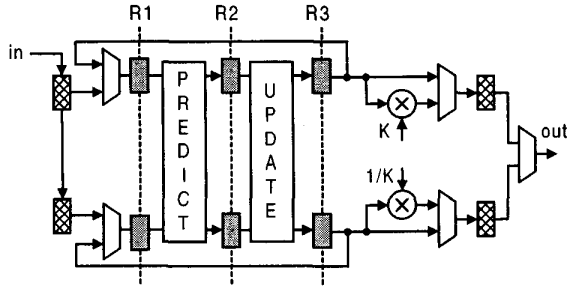

Fig. 5. Simplified block diagram with pre- and post- data formatter

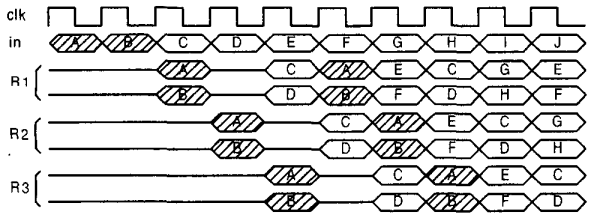

Fig. 6. Interleaving computation concept of the two stage operation in 9/7 filter mode

Being a dedicated DWT core for JPEG2000, the filter coefficients are fixed. Multiplications can therefore be further optimized. Hardwired multipliers are used instead of real multipliers to achieve a more compact design. The finite-precision coefficients are chosen to be within reasonable error range. Also, they are represented in their CSD [11] form to reduce the number of nonzero digits. Fewer nonzero digits mean fewer adders. Table IV shows the four coefficients represented in 12-bit CSD form.

Table IV
Filter coefficients represented in CSD form

	value	12-bit CSD representation	No. bits
α	1.586134342	$2^{1}-2^{-1}+2^{-3}-2^{-5}-2^{-7}+2^{-12}=1.5861816$	6
β	0.052980118	$2^{-4}-2^{-7}-2^{-9}+2^{-12}=0.0529785$	4
γ	0.882911076	$2^{0}-2^{-3}+2^{-7}=0.8828125$	3
δ	0.443506852	$2^{-1}-2^{-4}+2^{-7}-2^{-9}+2^{-12}=0.4436035$	5

3.2 2-D DWT Architecture

The computation style of the entropy coder after DWT will affect the optimal scheduling of the 2-D DWT computation. Fig. 7 shows the simplified JPEG2000 functional block diagram. Embedded Block Coding with Optimized Truncation (EBCOT) [13] is a block-coding engine. Images after DWT are decomposed into many sub-bands. Every sub-band is then partitioned into code-blocks. EBCOT processes these quantized wavelet coefficients code-block by code-block. After Tier-1 compression of EBCOT, every code-block will generate a sub-bitstream.

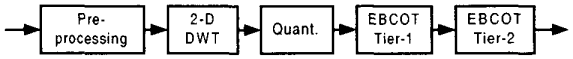

Fig. 7. Simplified JPEG2000 functional block diagram

To extend the 1-D DWT core to compute 2-D DWT in JPEG2000, two cases are considered. First, if a frame memory is necessary and has already existed before DWT operation. The data of the whole image are assumed to be stored in the memory. Although 2-D DWT can be scheduled to calculate all rows first (horizontal 1-D DWT), and then all columns (vertical 1-D DWT), it is possible to start the EBCOT computation once there is a complete code-block data available. Due to the in-place computing capability of lifting scheme, the original samples can be replaced directly by the calculated coefficients. Hence, the original frame-size memory is enough. The advantage of this implementation is the ease of data flow control. Due to the interleaving characteristics of the output, i.e., one low pass sample followed by one high pass sample, the interleaving storage arrangement is illustrated by an example of a 4×4 image show in Fig. 8. An address generator (AG) is needed to provide the proper access addresses to read samples for next level wavelet decomposition and then write back. The block diagram of the JPEG 2000 system is shown in Fig. 9. The frame memory is used for the storage of the data for DWT, and also for the entropy coded sub-bitstreams of each code-block after EBCOT.

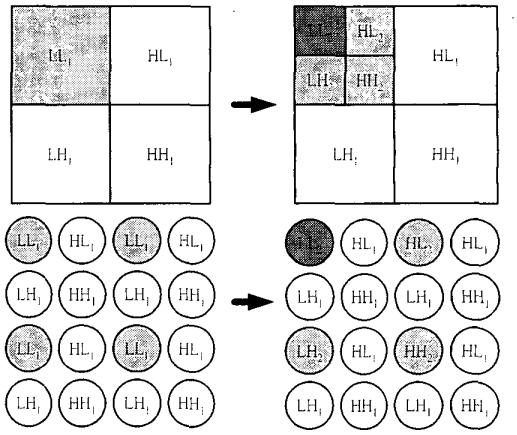

Fig. 8. Example of 2-level wavelet transform shows the in-place interleaving organization of wavelet coefficients, where a circle represents a pixel.

Second, if a frame memory is not available or not allowed due to the constraint on the cost of the memory size. Then, the concept of line-based DWT [12] can be adopted. Since EBCOT is not line-based, the height of the line buffer will depend on the height

of the code-block. The required buffer size for DWT will be smaller than the frame memory. However, another memory space for the compressed sub-bitstreams of every code-block is necessary.

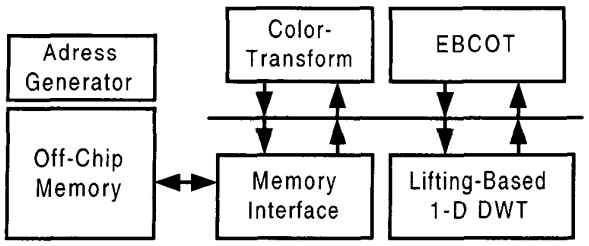

Fig. 9. JPEG 2000 system block diagram

4. CONCLUSION

A re-configurable lifting based 1-D DWT core is proposed in this paper. Folded architecture is adopted to reduce the hardware cost and to achieve the higher hardware utilization. Multiplication is realized in hardwired multiplier with coefficients represented in CSD form. It is a compact and efficient DWT core for the hardware implementation of JPEG2000 encoder. The future work will be the optimization of the scheduling and memory organization of the overall JPEG2000 system.

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